ELECTENG311

Part 3

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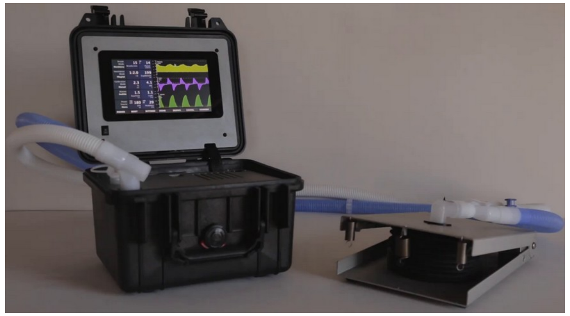
(Based on notes prepared by Dr Jackman F.Y. Lin (2021))

About Matthew

- PhD UoA Completed 2020, Inductive Power Transfer Magnetics for Roads
- Post Doc, Tennessee Tech University 2021-2022, Single contact CPT and Through the Soil Power Transfer
- Post Doc, UoA, 2022, Motor Drives for Superconducting Electric Motors.



Practical Considerations

Practical Considerations – Learning Objectives

By the end of this lecture students will understand

- Practical limits of a flyback converter
- Additional circuitry for more efficient and practical operation
- Using standard laboratory equipment to test for circuit failures
- Practical limitations of different types of capacitors

Practical Considerations – Revision

- So far you have learned:
    - Flyback converter topology theory and design
    - Control of flybacks
        - Open loop
        - Closed loop – PI
    - Using the UC3843 controller
    - MOSFETs
    - Magnetics
    - Transformer design
    - Leakage inductance
    - Component selection
    - Isolation

Today

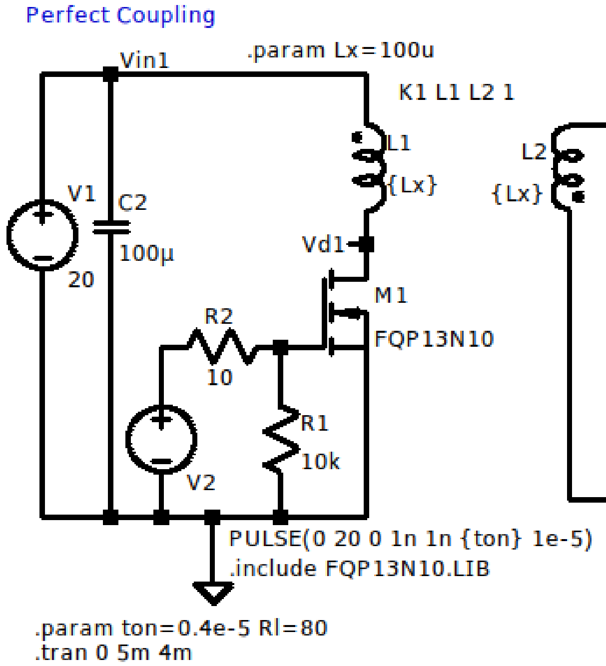
- Overshoots and Ringing
  - Leakage Inductance
  - Parasitic Capacitance
  - FET Avalanche Mode
  - Snubbers
- Thermal Management
- Circuit Debugging (Test Equipment)
- Practical Capacitors

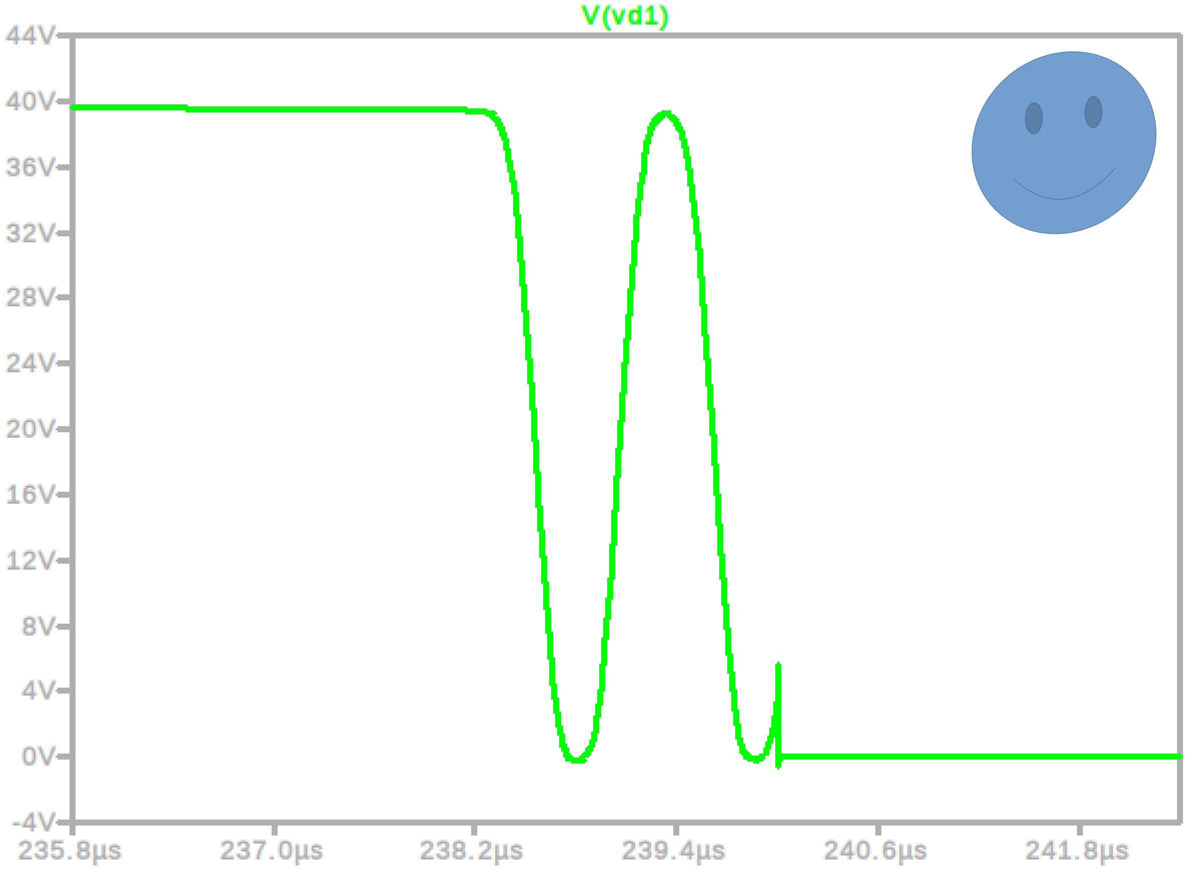
Practical impacts of FETS and Leakage Inductance

Or "Sometimes we get some components for free!"

Overshoots and Ringing – Example

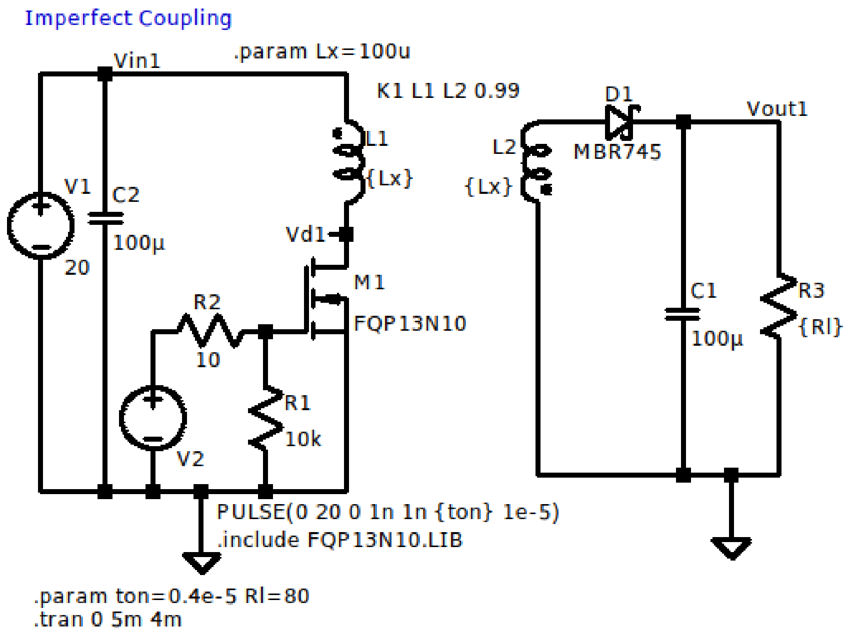
- Perfect inductor (Discontinuous mode)
  - Practically impossible (k = 1)
- No overshoots – great!

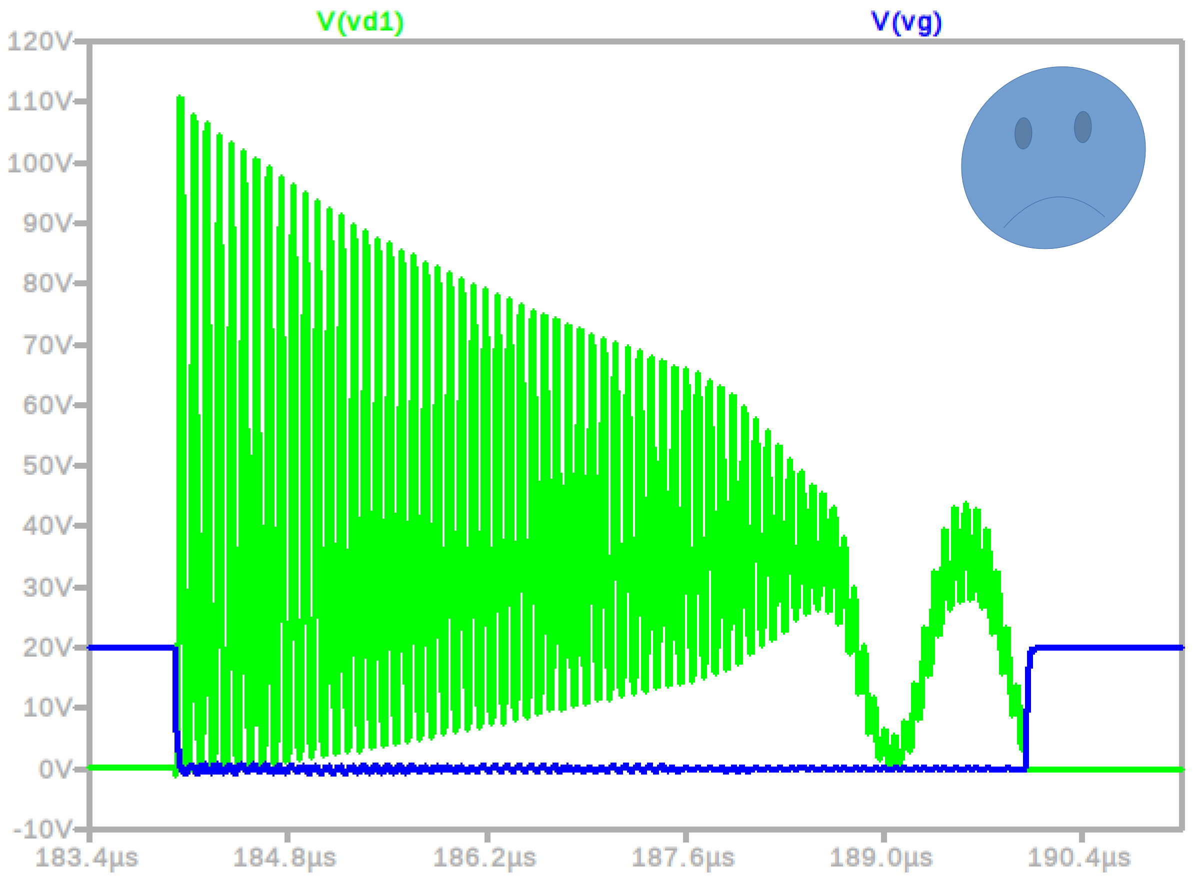




Overshoots and Ringing – Example

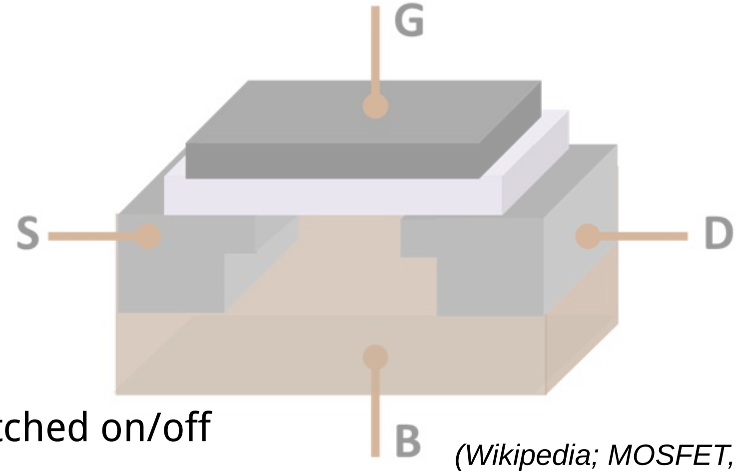
- A very good inductor (yours?) (k = 0.99)
- Uh-oh!
  - Overshoot up to 110 V
  - Excessive ringing on the switch
  - Occurs when the switch turns off





Overshoots and Ringing – Parasitic Capacitances

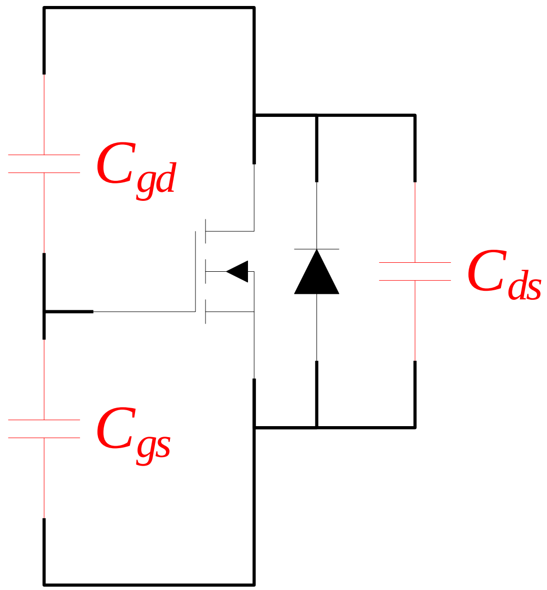
- MOSFETs have parasitic capacitances because of the way they are constructed:
  - $C_{iss} = C_{gd} + C_{gs}$
  - $C_{oss} = C_{gd} + C_{ds}$
  - $C_{rss} = C_{gd}$
- These dynamic characteristics have a big impacts on circuits when they are switched on/off
- FQP13N10 has a table of typical and maximum parasitic values under certain operating conditions
- These are also why we need a high MOSFET drive current!



(Wikipedia; MOSFET, Brews ohare)

Dynamic Characteristics

C_{iss}	Input Capacitance	V_{DS} = 25 V, V_{GS} = 0 V, f = 1.0 MHz	--	345	450	pF
C_{oss}	Output Capacitance		--	100	130	pF
C_{rss}	Reverse Transfer Capacitance		--	20	25	pF



Leakage Inductance and Parasitic Capacitance

- The leakage inductance (L_{lk}) and parasitic capacitance (C_{oss}) cause ringing
- Ringing occurs when the switch turns off from an on state
  - Caused by Coss of the MOSFET
  - Modelled as a lumped capacitor across drain-source for simplicity

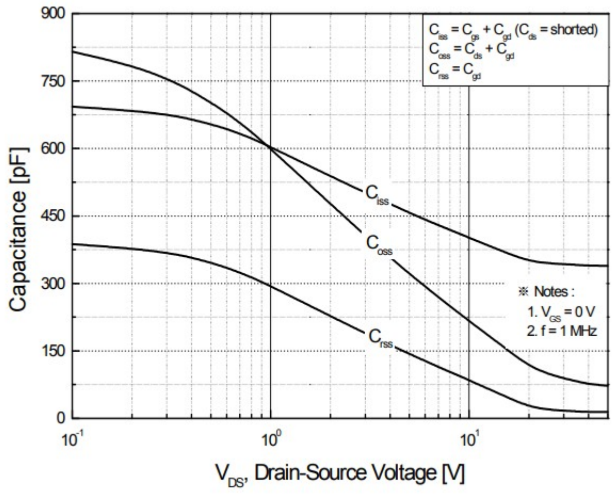
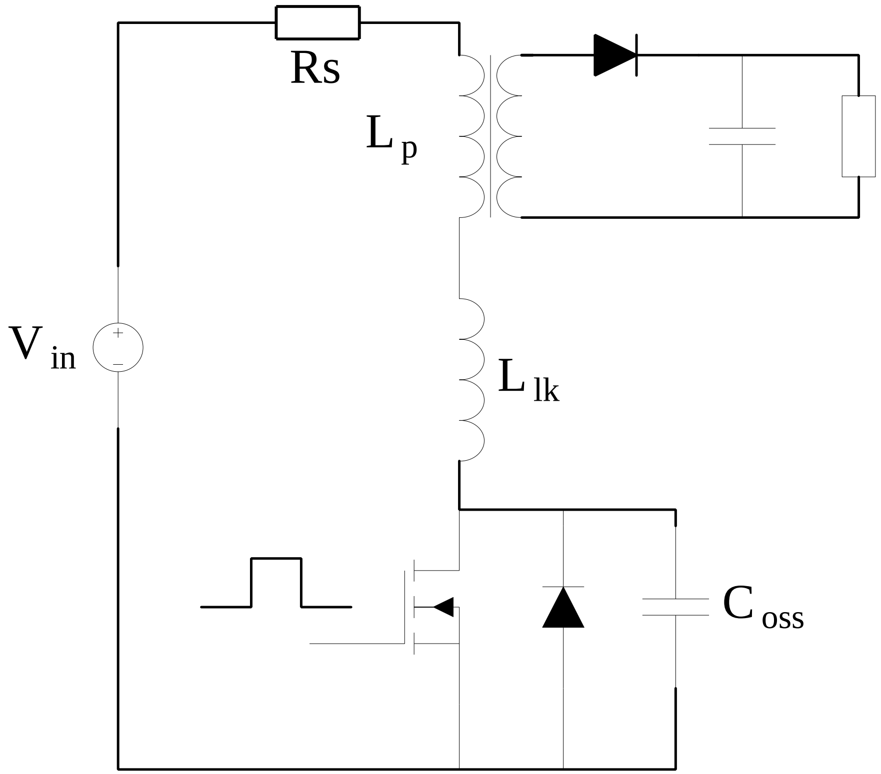
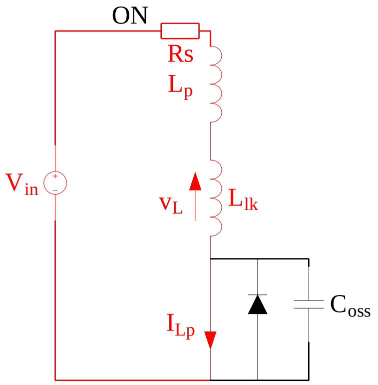


Figure 5. Capacitance Characteristics



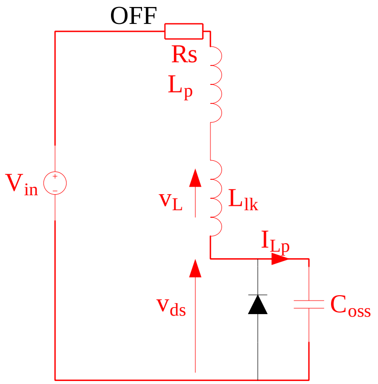
- **Try:**
  - **Perform an Ltspice simulation of a flyback converter with an ideal switch (Coss = 0) and coupling factor = 0.99.**

Overshoots and Ringing

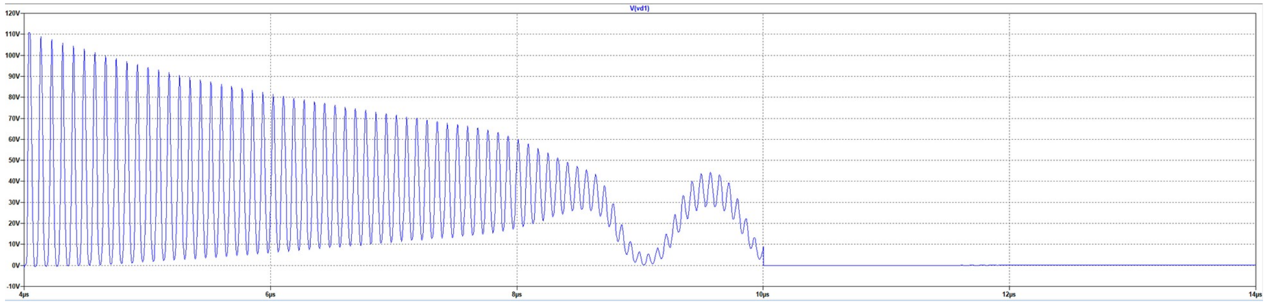


- When the switch is on:
  - Leakage inductance charged to a certain energy based on the on time.

$$E = \frac{1}{2}LI^2$$

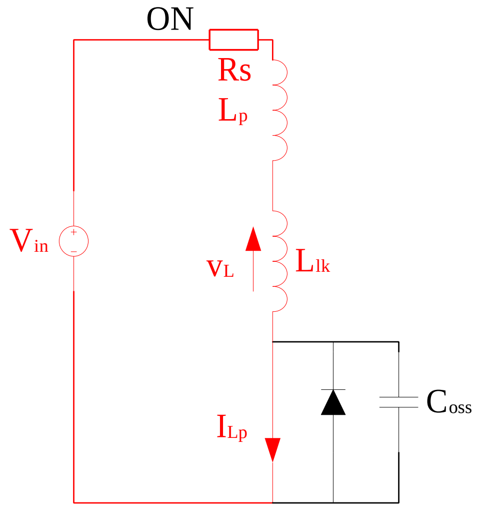


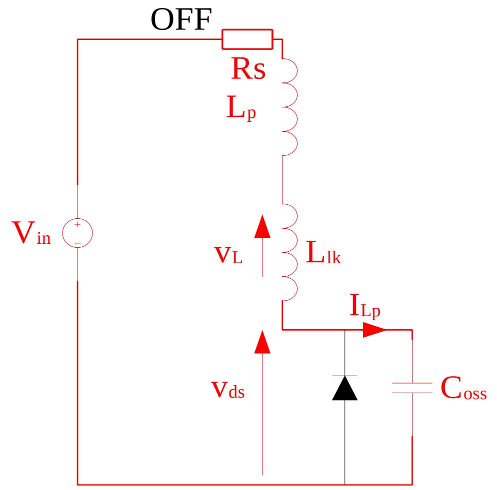
- When the switch is turned off:
  - The energy in the magnetizing inductor is dissipated in the output capacitor (not shown)
    - The output voltage reflects onto the primary side.
    - $V_{ref} = n(V_{out} + V_f)$, where $n = \frac{N_p}{N_s}$
    - V_f is the forward voltage of the output diode
  - The energy in the leakage inductor must also be dissipated somewhere
    - Through the output capacitor
  - After all the energy is dissipated:
    - Magnetizing inductance comes into play
    - Lower frequency ringing is observed



Overshoots and Ringing

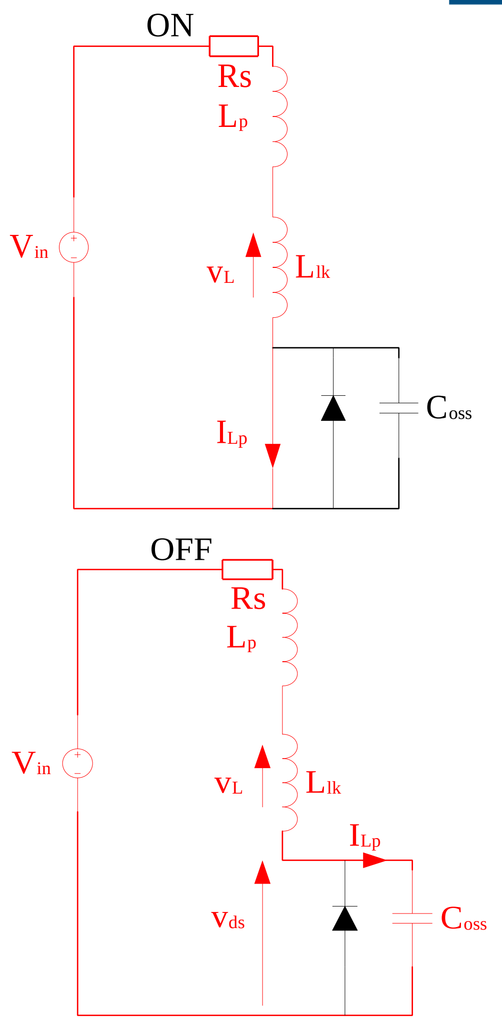
- The current in an inductor cannot change instantaneously $v_L = L\frac{di}{dt}$
  - At the switching instant, the current in the leakage inductor is maximum
- The voltage across a capacitor cannot change instantaneously $i_c = C\frac{dv}{dt}$
  - At the switching instant, the voltage across the capacitor is almost 0
- When the switch turns off, the current in the system is suddenly forced into the output capacitor of the switch
  - Energy is conserved: $\frac{1}{2}LI^2 = \frac{1}{2}CV^2$
  - $V = I\sqrt{\frac{L}{C}}$, where I is the peak current at the switching moment
  - This causes a large voltage spike across Coss
  - Typically, we can approximate Vds as: $$V_{ds} = V_{in} + V_{ref} + I_{Lp,peak}\sqrt{\frac{L_{lk}}{C_{oss}}}$$
  - Note that this equation only assumes an ideal switch with only Coss (which varies with Vds)
    - Real switches and circuit board will have other parasitics!





Overshoots and Ringing – What's going on here?

- But wait! In the previous example we had:
  - $V_{in} = 20\ V$
  - $D = 0.4$
  - $f = 100\ kHz$
  - $L_{lk} = 1.99\ \mu H$
  - $C_{oss} = 100\ pF$
  - $V_{out} = \sqrt{\frac{R_L}{2 f_s L_p}} * V_{in} D = 16\ V$
  - $I_{Lp,peak} = \frac{V_{in}}{L_p} D T_s = 0.8\ A$
- So Vds should be $\mathrm{Vds} = 20 + 1 * (16 + 0.7) + 0.8\sqrt{\frac{L_{lk}}{Coss}} = 149.55\ \mathrm{V}$
- Why does the simulation cap out at 110 V?
- This zone is called the Avalanche mode



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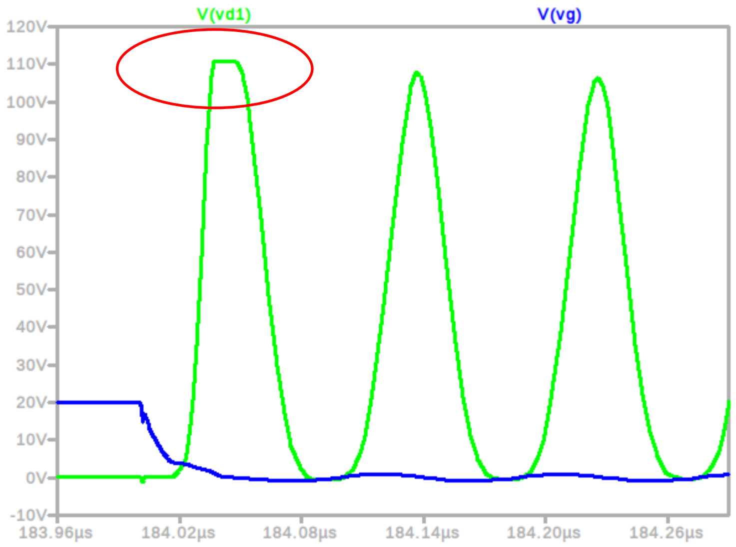

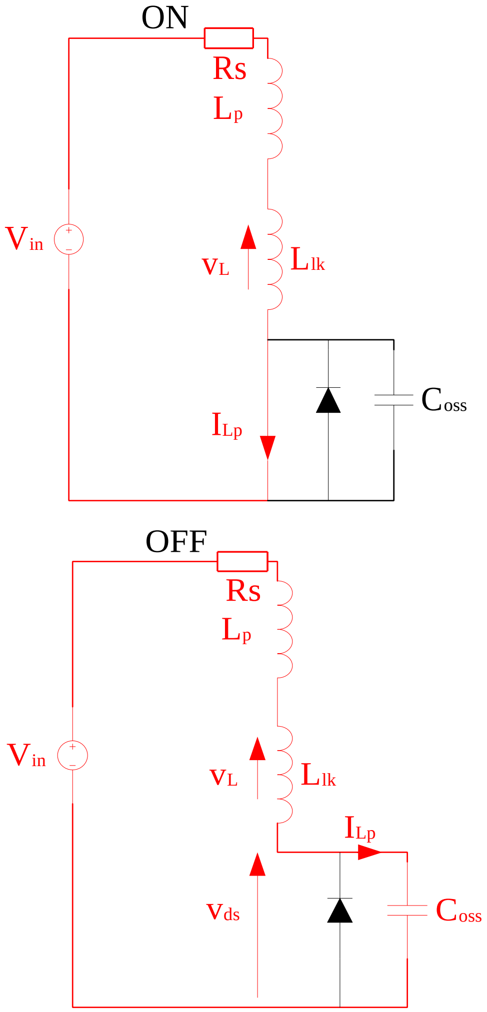

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Avalanche Mode Operation

- Avalanche mode occurs when the voltage across the MOSFET exceeds the maximum rated voltage as stated in the datasheet:
  - For the FQP13N10 the BVdss (Breakdown Vds) is 100 V
  - The FQP13N10 is rated for avalanche breakdown
    - **Not all FETS are**
- In avalanche mode, the FET behaves like a Zener Diode
  - Clamps the voltage at 110 V
  - Not always 10% higher than Rated BVdss
    - Check the datasheets for all your switches
- Excess energy is dissipated as heat, and *can be destructive*

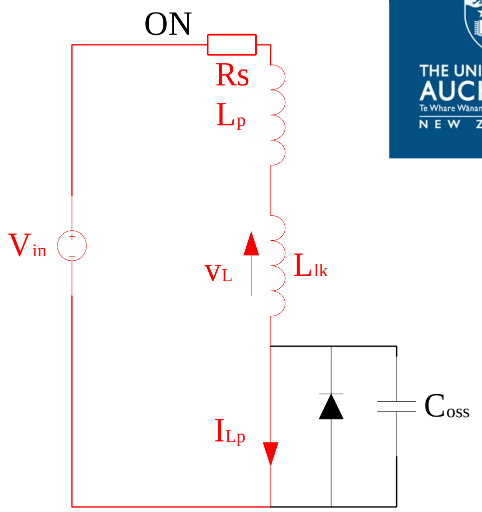
(Wikipedia: Avalanche: Chagai)

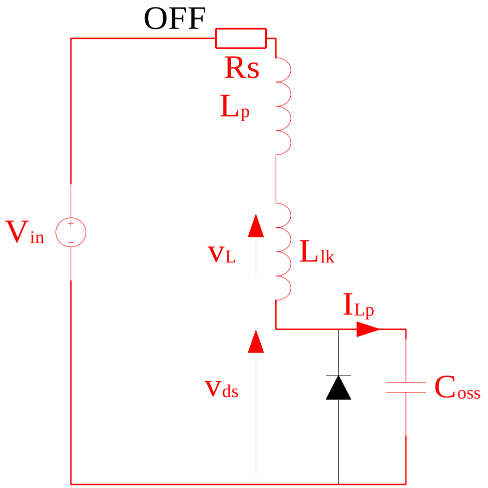
Avalanche Mode Operation

- Avalanche constraints are in the datasheet
- On switching edge, the energy dissipated in the FET is equal to the energy stored in the leakage inductance of the transformer

$$E = \frac{1}{2}LI^2$$

- At $I_{Lp,peak}$ = 800 mA, and a coupling factor of 0.99, the avalanche energy is approximately 0.4 μJ < 6.5 mJ
- Note that for *your* project your Avalanche energy will depend on:
    - Your power rating
    - Your transformer design
- Since you will be pulsing Vds frequently, use the *repetitive avalanche energy rating*
- **Try: Perform an LTSpice simulation and replace the MOSFET with an ideal switch with an output Coss with k = 0.99. Confirm that the Vds spike reaches approximately what is calculated for a switch without avalanche.**





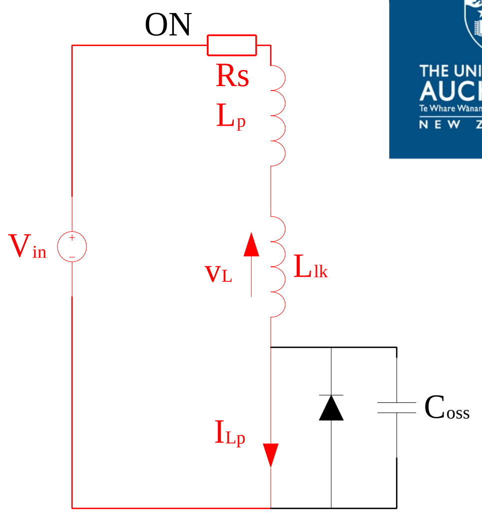
E_{AS}	Single Pulsed Avalanche Energy	(Note 2)	95	mJ
I_{AR}	Avalanche Current	(Note 1)	12.8	A
E_{AR}	Repetitive Avalanche Energy	(Note 1)	6.5	mJ

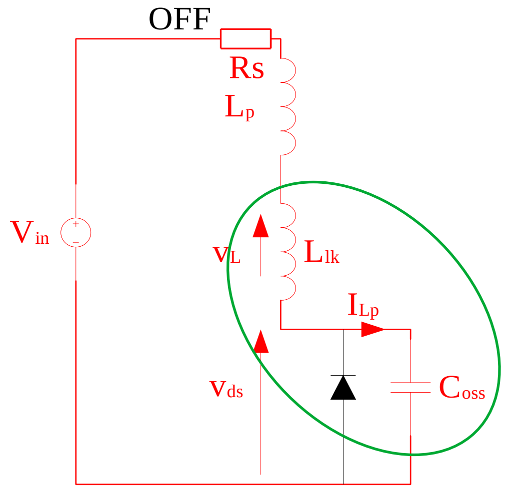
Ringing Frequency

- We can also see that when the switch turns off there is now an LC circuit
  - Formed by the leakage inductance and the output capacitance
  - An ideal LC circuit has a ringing frequency given by:

$$f = \frac{1}{2\pi\sqrt{LC}}$$

  - Where L is the leakage inductance (L_{lk}), and C is the parasitic capacitance of the entire circuit (not just Coss)
- **Try:**
  - **Using LTspice, show that the ringing frequency relates to the leakage inductance and Coss of a switch by setting up a simulation with an ideal switch, an output Coss = 100 pF, and a coupling factor of 0.99. Use a variety of Lp values to show that the ringing frequency changes**





Managing Overshoots and Ringing

- Overshoots and ringing lead to excess loss in the circuit
- EMI issues also occur

- Practical methods of managing/minimizing the overshoots and ringing include:
  - Snubbers
  - Voltage clamps
  - Active clamps
- We will only cover snubber design

- You will be expected to design your own snubbers as a minimum requirement in this course.
- You are allowed to use other overshoot and ringing management techniques
  - Provided you can prove that you have designed it properly!

Snubbers

- A well designed snubber circuit reduces the ringing of the Vds on the switching edge
- An RC circuit across the transformer will achieve this goal.
  - RC circuit gives the leakage energy in the transformer another path to flow
  - Values for R and C need to be chosen carefully!
    - Improperly designed snubbers will result in even more loss than no snubber!

- Design steps:
  1. Extract ringing frequency (f_r) and the leakage inductance (L_{lk}) information from simulation/measurements
  2. Set a resistance R which is equal to the impedance of the leakage inductance:

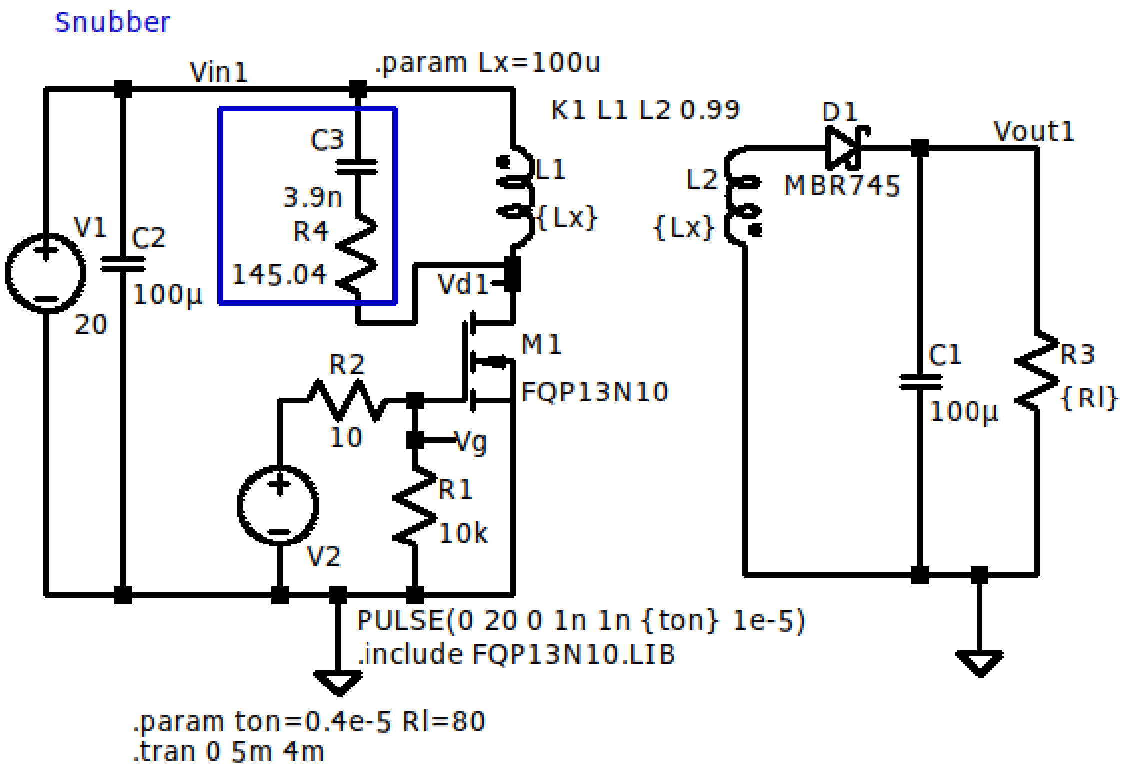
     $$R = 2\pi f_r L_{leak}$$

  3. Set impedance of C equal to this resistance

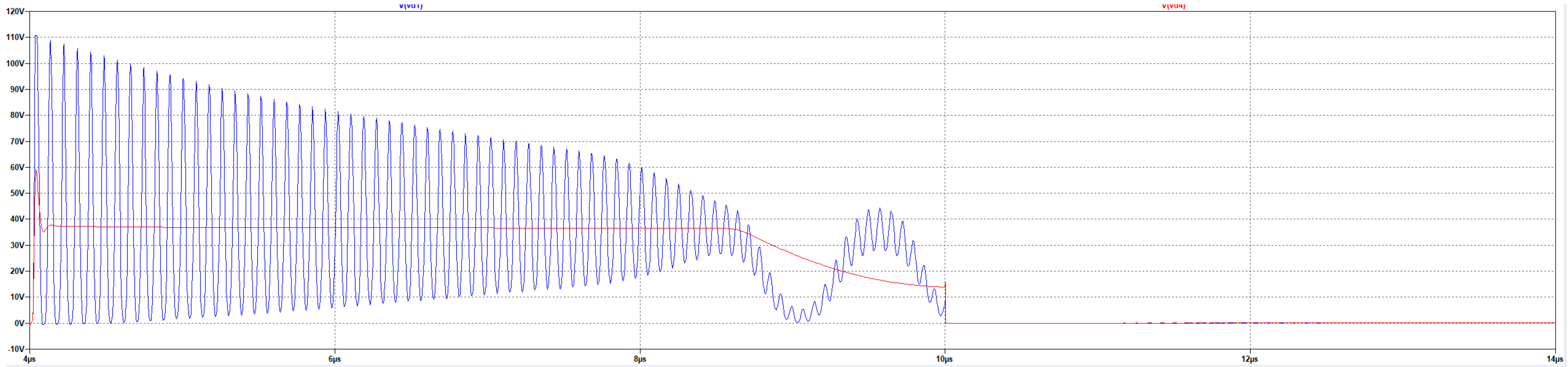
     $$C = \frac{1}{2\pi f_r R}$$

Snubbers – Example

- Example:
  - Lp = 100 µH
  - k = 0.99
  - FQP13N10 MOSFET
  - R_L = 80 Ω
  - D = 0.4
- L_{leak} = 1.99 uH, $f_r \approx$ 11.6 MHz, (from simulation) (11.3 MHz from calculation)
- Calculate R = 145.04 Ω using simulation values
- Calculate C = 3.7 nF

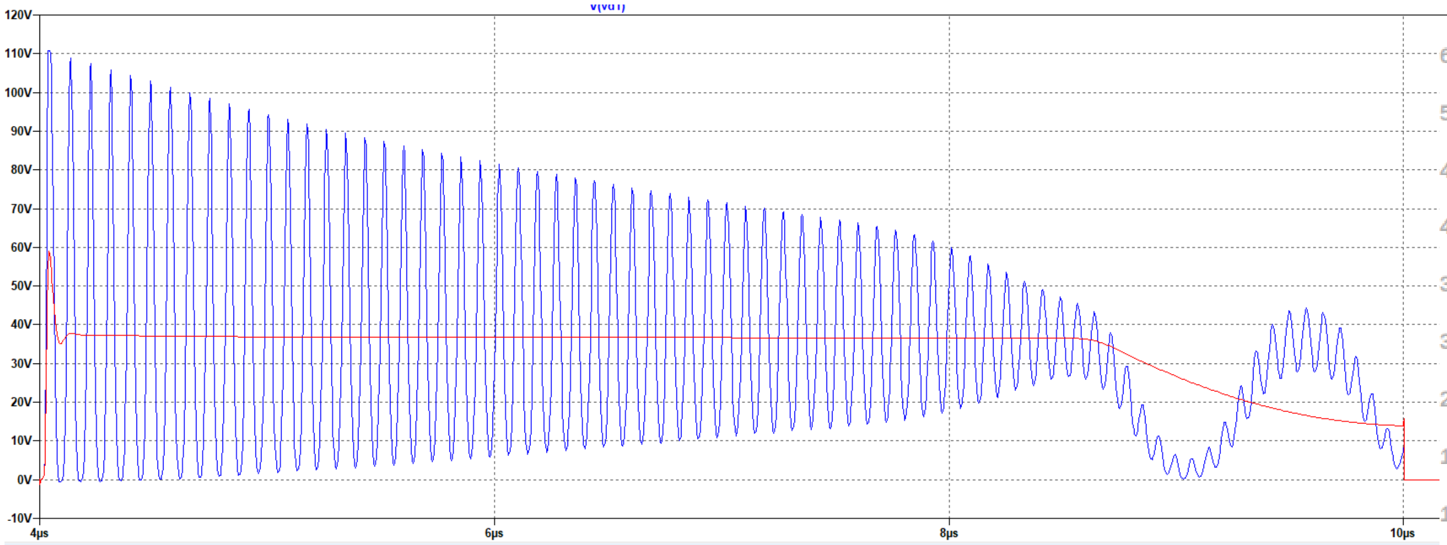


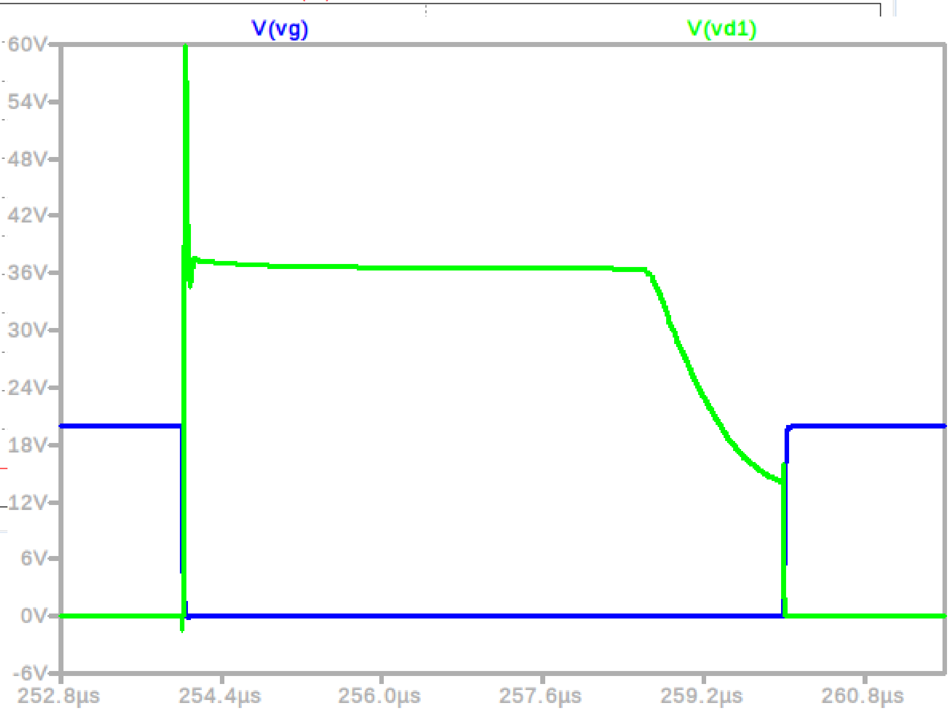
Snubbers – Effective



- Too good to be true?
  - Peak voltage is lower – down from avalanche mode to 60 V peak
  - Almost no ringing
- Snubber circuit also has losses
  - If the circuit layout has different parameters then the snubber resistor will have excessive loss
  - Could end up being less efficient than a snubber-less circuit

Snubbers – Effective





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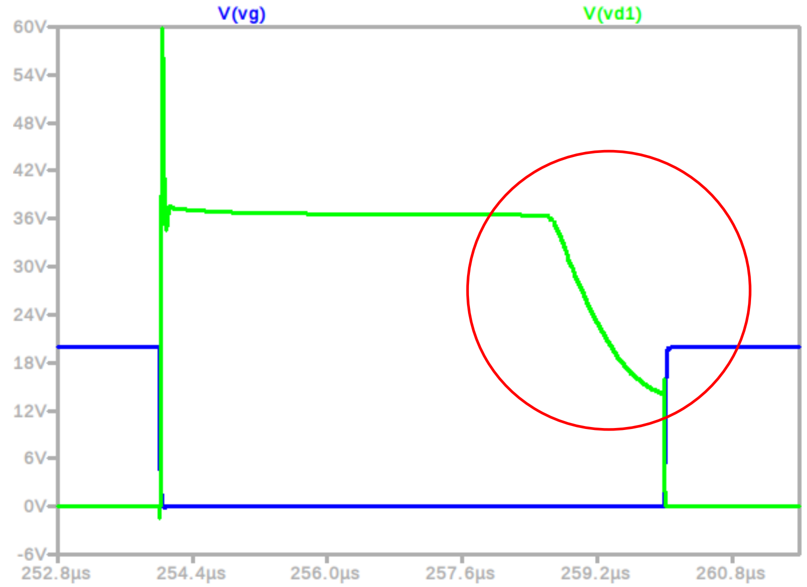
Snubbers – Power Loss (the trade-off)

- The power loss in the snubber resistor is determined by
  - If the snubber is designed to be (virtually) perfect then when the switch turns off, all of the energy in the inductor is shunted into the resistor
  - If the converter has a lot of energy in the leakage inductance then your converter efficiency will decrease
  - Need to increase R and decrease C to lower losses
    - Higher R
  - You will trade off efficiency for ringing
- Practical values for your snubber circuit will also have an impact on how well you can design the snubber itself
  - You're never getting a 145.04 Ω resistor
- This simulation is only for one operating condition, you will need to consider your worst case operating condition.

- **Questions:**
  - How far can you increase R or decrease C before the snubber loses effectiveness?
  - What do you consider acceptable?
  - Is the snubber realizable?

Snubbers – More complex designs



- The proposed snubber design only reduces ringing for the high frequency components
- Low frequency oscillations still occur after the energy in the leakage inductance is dissipated
  - Frequency is related to the magnetizing inductance and the snubber circuit
- Low frequency ringing can also be reduced through a more advanced snubber design
  - RCD snubbers
  - Active clamps

Thermal Management

Thermal Management – Thermal Resistance

- How hot will your FET get?
- Datasheet for the FQP13N10 has the data shown

Thermal Characteristics

Symbol	Parameter	FQP13N10	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case, Max.	2.31	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient, Max.	62.5	°C/W

- If no heatsink is used, then use *Junction-to-Ambient* resistance
- For every watt of power dissipated in the switch, the FET will rise 62.5 degrees above ambient (usually 25 °C)
- According to datasheet, FET has an absolute maximum operating temperature of 175 °C

Thermal Management – Heatsinking

- If the switch reaches 175°C it will fail
- You may find that you will need a heatsink for your design
- If you do, then we use the *Junction-to-Case* thermal resistance
- When using a heatsink we need to use thermal compound to ensure good contact between the FET and the Heatsink (fill in air pockets)
    - Thermal compound has its own thermal resistance
        - Typical compounds have $R_{\theta TC}$<0.25 °C/W
    - Heatsinks also have a case to ambient thermal resistance ($R_{th,HS}$)
        - Example heatsink has $R_{\theta HS}$ = 25 °C/W
- Total Rth = $R_{\theta JC} + R_{\theta TC} + R_{\theta HS}$
    - Example: Rth = 2.31 + 0.25 + 25 = 27.56 °C/W if the FET is mounted to the heatsink using a thermal compound with Rth = 0.25 °C/W.
    - Even lower if a fan is used
    - Fans add cost

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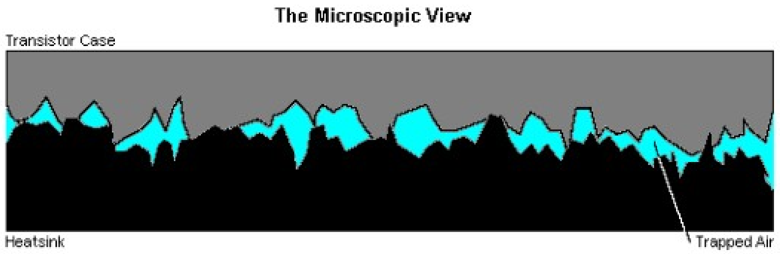
Example Heatsink Parameters

Thermal Performance at Typical Load

Natural Convection	Forced Convection
50°C @ 2W	9.0 C/W @ 400 LFM
50°C @ 2W	9.0 C/W @ 400 LFM
44°C @ 2W	7.0 C/W @ 400 LFM
44°C @ 2W	7.0 C/W @ 400 LFM

http://www.wakefield-vette.com/Portals/0/resources/datasheets/289,290.pdf



https://sound-au.com/heatsinks.htm

Circuit debugging

Testing your circuit

- During circuit testing you will probably end up unsure if certain components still work!
- Methods to test:
  - You have access to oscilloscopes, waveform generators, and multimeters
  - You will need to be able to use both for this project
    - There are dc and ac / analogue and digital signals to measure
    - Use the right tool for the right task

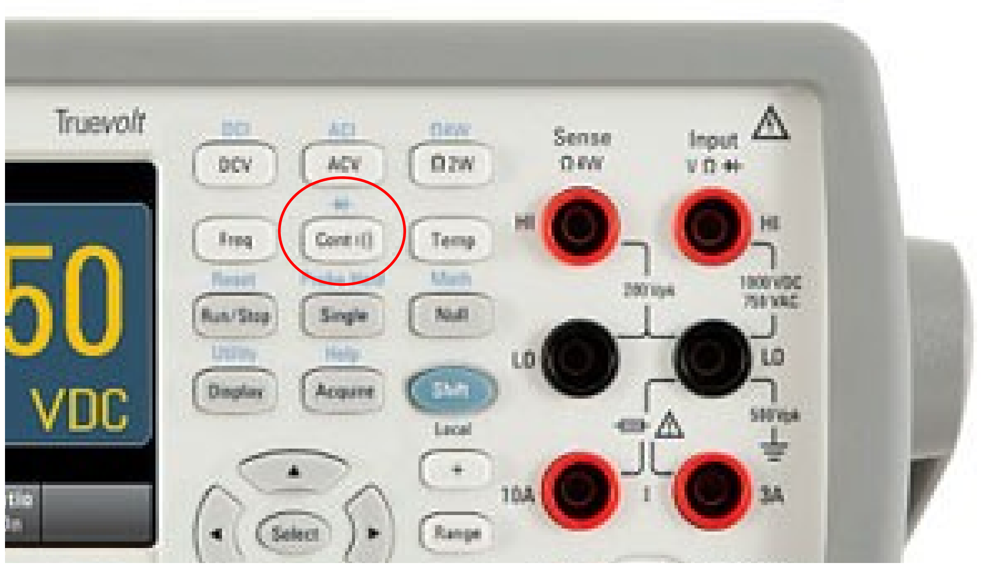
https://www.hioki.com/global/products/testers/dmm-4/id_5803

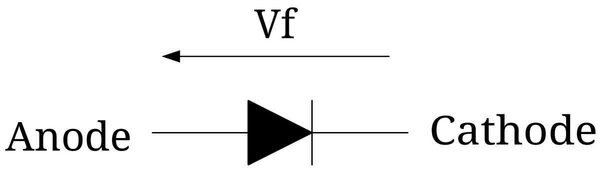
Testing a Diode

- Using a multimeter to test a diode
  - Select diode test feature
- Features to test:
  - Diodes should block current flow if connected backwards
  - If a diode is working, then it should have a forward voltage drop (Vf)

    $$Vf \approx 0.7V$$

    - Check your datasheets

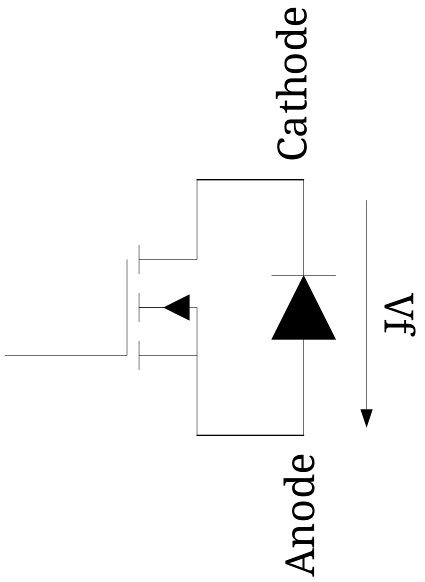




- Test procedure:
  1. Ensure your circuit is not powered
  2. Make sure the leads are connected properly
     a) Quick continuity test
  3. Place the red lead on the Anode and the black lead on the Cathode
     a) Measure the forward voltage drop
  4. Reverse your leads (black on cathode, red on anode)
     a) Measurement should show open circuit

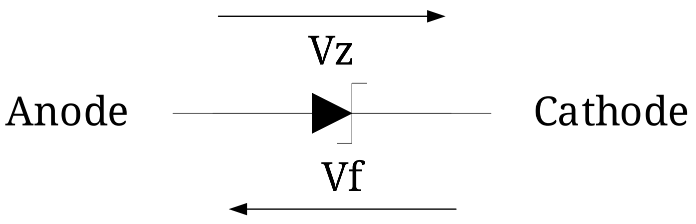
Testing a FET

- So, you think your FET has failed
  - How do you test it?
- Normally when a MOSFET fails the internal silicone fuses together and it becomes short circuited
- Remember that the FQP13N10 is a MOSFET with a body diode.
- Use the diode option on the multi-meter
  1. Ensure your circuit is not powered
  2. Place the positive end on the anode
  3. Place the negative end on the cathode
     a) If there is a voltage drop then the body diode is fine
  4. Reverse the connections
     a) If the circuit shows an open circuit, then your MOSFET is most likely fine
  5. Place a dc voltage across the drain-source of the MOSFET
  6. Drive the MOSFET with an artificial pulse from the waveform generator

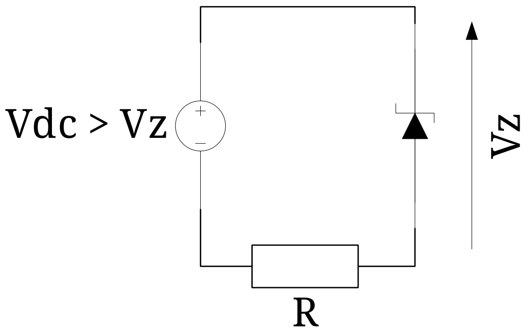


Testing a Zener Diode

- Zener diodes constrain the voltage between the anode and cathode
- Zeners have a forward voltage and a Zener breakdown voltage
- To test the forward voltage, follow the same steps as [Testing a Diode]



- To test the Zener Voltage, you need to set up (at the minimum) the circuit shown:
    1. Set up the resistor so that the Zener diode does not get too hot!
    2. Increase your dc supply voltage so that it is higher than the Zener Voltage
    3. Measure the voltage across your Zener diode and make sure it equals what is expected



Capacitor Selection

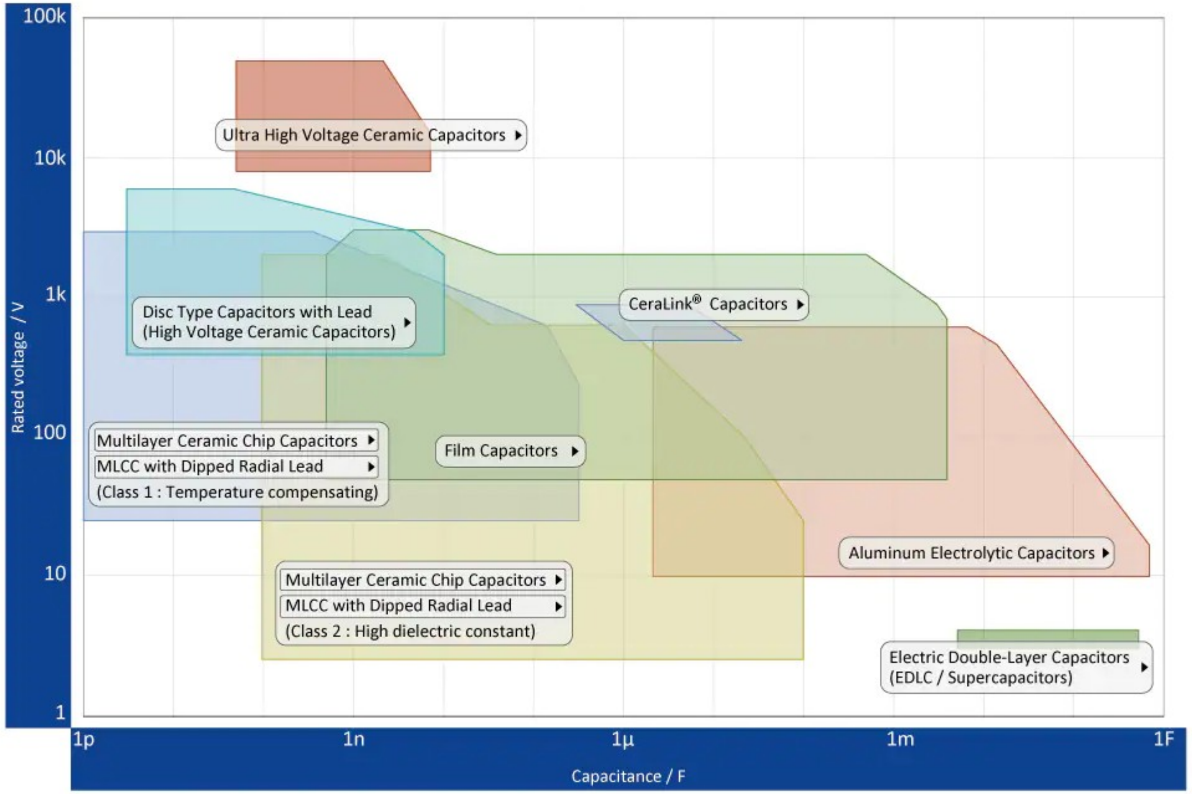
Capacitor types

- Previously you have learned about different types of capacitors
  - Electrolytic
    - Usually for dc links
    - High energy storage
    - Limited lifetime
    - Placement needs care to avoid operating at high temperatures
  - Film
    - Used for dc links and decoupling
    - Limited lifetime
    - Lots of different methods of construction/dielectric material
  - Ceramic
    - Used for resonant circuit and decoupling
    - Lots of different methods of construction/dielectric material
- The requirement for this project is for a compact dc-dc converter
  - Therefore, the use of electrolytic capacitors is minimized, but cannot be avoided

(Wikipedia, Capacitor: Eric Schrader)

Capacitor Types

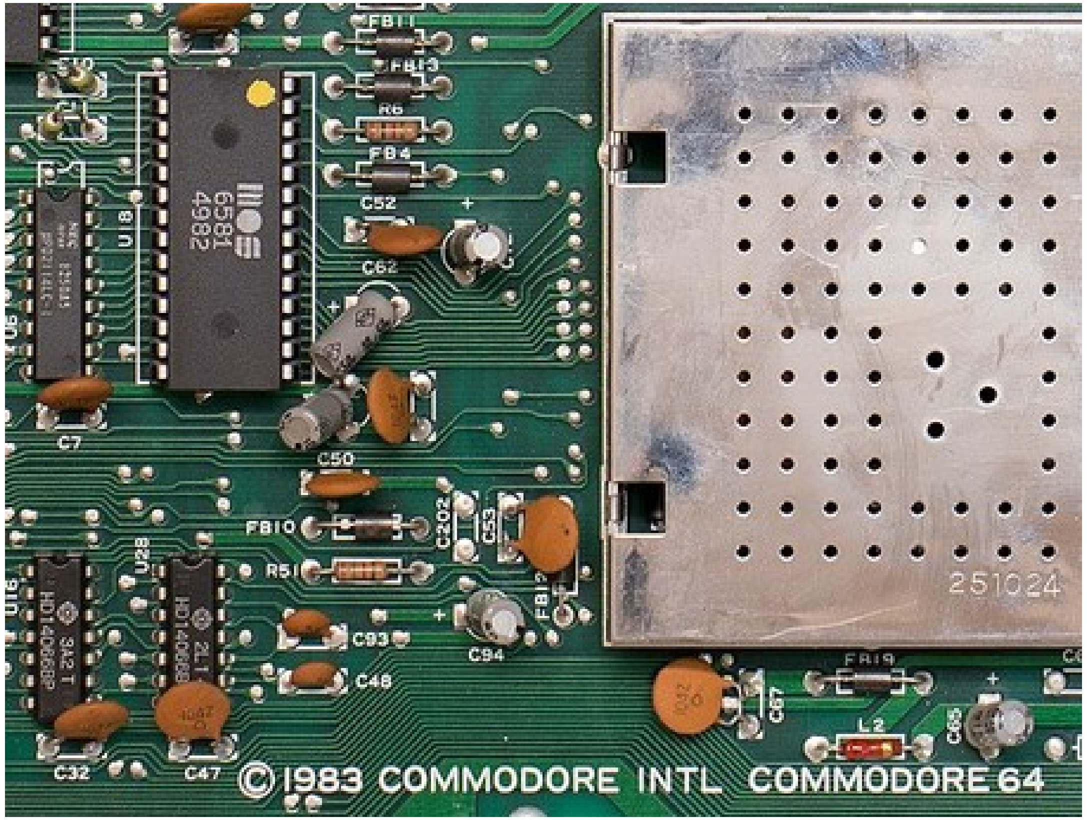
- Different types of capacitors will have different applications
  - High frequency tuning
    - Low capacitance, low/high voltage
      - Ceramic and film
  - Dc-link capacitors
    - High capacitance, high voltage
      - Electrolytic, film, power
  - Decoupling capacitors
    - Low capacitance, low voltage
      - Ceramic and film
  - Energy storage
    - High capacitance, low voltage
      - Super-capacitors



https://product.tdk.com/en/products/selectionguide/capacitor.html

Decoupling Capacitors

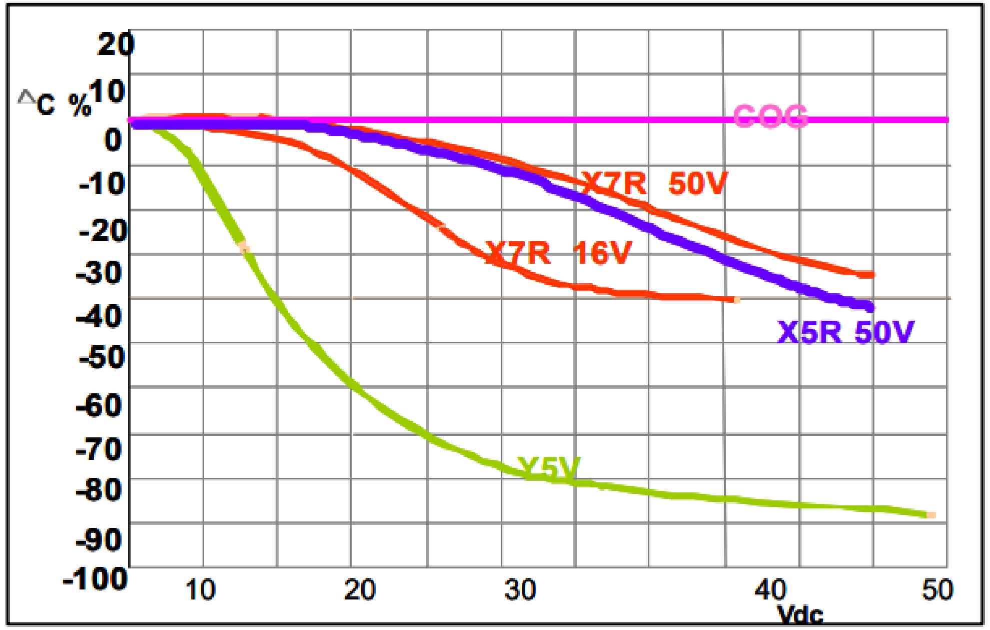
- Decoupling capacitors shunt noise to ground
- Also can be thought of as a local energy store
- (don't confuse with coupling capacitors, which are for blocking DC between AC stages)
- Typically placed as close as possible to ICs to minimise the supply line inductance and series resistance
- A combination of types is often used as capacitors differ in high-frequency characteristisc
- Typically something of the order of 10-100 uF Electrolytic and several 100 nF ceramics placed close to the ICs



(*Wikipedia: Decoupling Capacitor: Sven.petersen*)

Capacitor Voltage Dependence

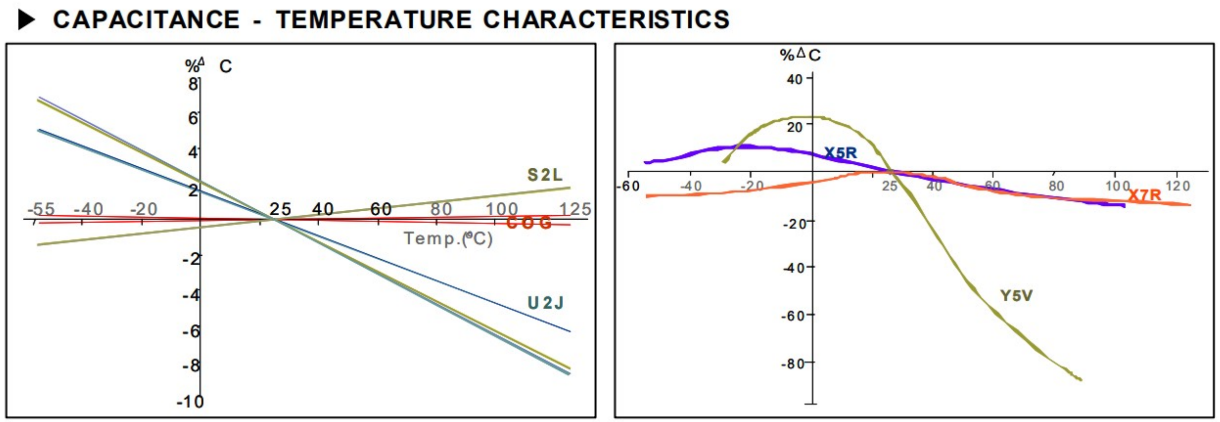
- There are lots of sub-categories for capacitors
  - Ceramic: C0G/NP0, X7R, Y5V
  - These are temperature coefficients
  - Determines how stable the capacitances are with respect to changes in temperature/voltage/frequency
    - High voltages/frequencies lead to high temperatures, so temperature coefficients are used to capture the big picture
- If capacitors are run near their maximum ratings, then the capacitance degrades
  - Mostly an issue with ceramic caps
- C0G/NP0 capacitors are great, but expensive.
- Information is in datasheets



https://www.tme.eu/Document/4a42202b32dab16128fe107dd69598cc/samsung-chip-cap.pdf

Capacitor Temperature Dependence

- Capacitance also changes based on temperature
  - Affects all capacitors
- C0G ceramic capacitors look great
  - Again, $$$



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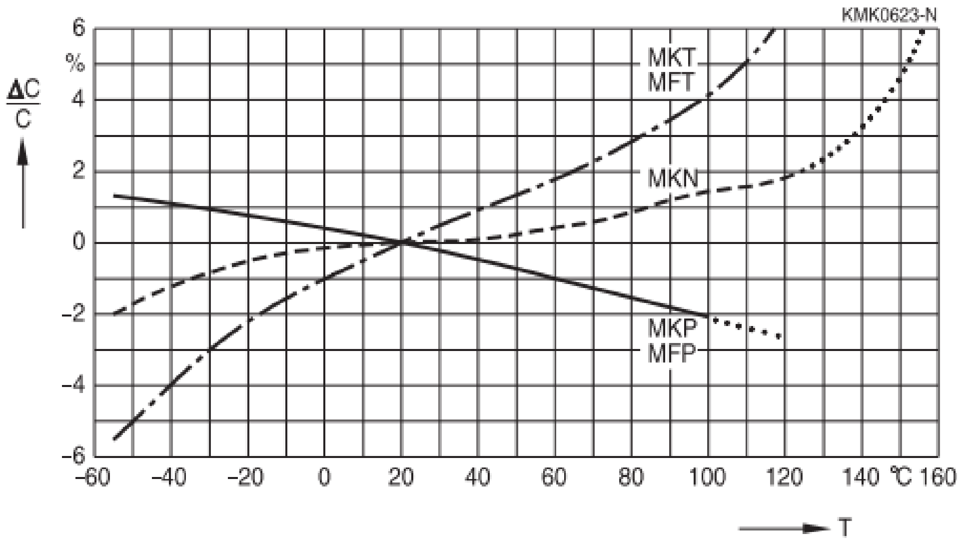


Figure 9
Relative capacitance change ΔC/C vs. temperature T (typical values)

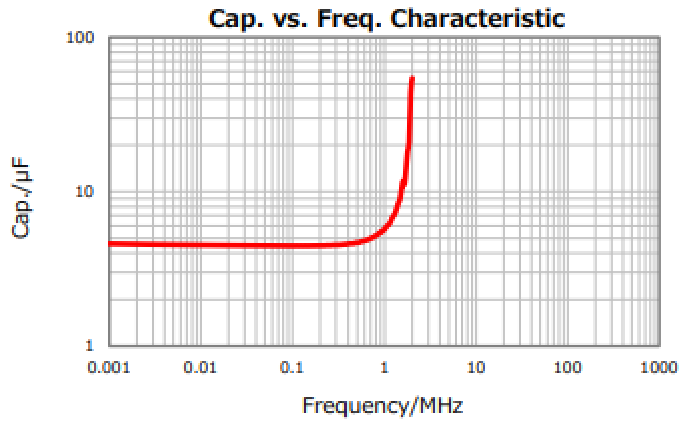
https://www.tdk-electronics.tdk.com/download/530754/480aeb04c789e45ef5bb9681513474ba/pdf-generaltechnicalinformation.pdf

Capacitor Frequency Dependence

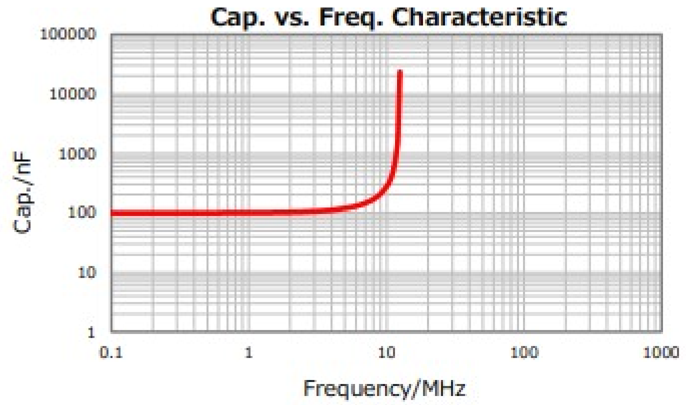
- Top Picture: X7R characterization sheet
- Bottom Picture: C0G characterization sheet

- C0G has an order of magnitude higher frequency stability than X7R
  - For these TDK capacitors

- C0Gs are great, but cost more



https://product.tdk.com/system/files/dam/doc/product/capacitor/ceramic/mlcc/charasheet/cnc6p1x7r2a475k250ae_210616.pdf

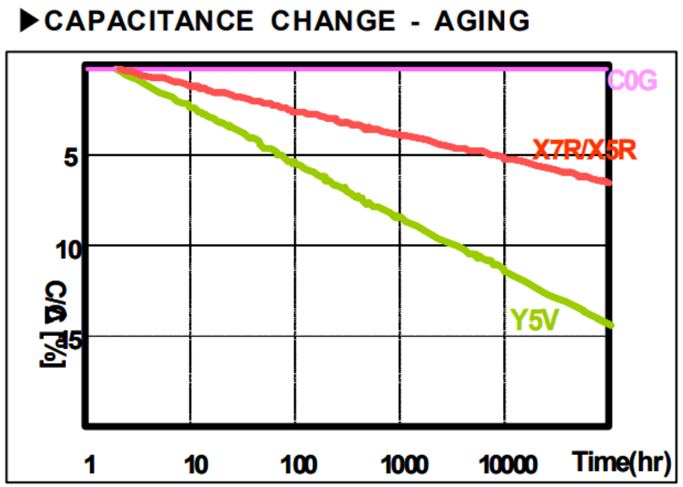


https://product.tdk.com/system/files/dam/doc/product/capacitor/ceramic/mlcc/charasheet/c5750c0g2j104j280kc.pdf

Capacitor Lifetime

- All capacitors have a finite lifetime
- Dependent on temperature
- If capacitors are placed near components that will get hot (i.e., a hot switch), then lifetime will decrease faster.

- Design for expected lifetime operation
- If you expect your product to last longer than the capacitor lifetime
  - Place more capacitors than required
    - Degradations will be compensated over time
    - More capacitors = less heat generations in each cap
- If the value of the capacitance is critical (i.e., high frequency tuning)
  - Consider paying more for C0G grade capacitors



https://www.tme.eu/Document/4a42202b32dab16128fe107dd69598cc/samsung-chip-cap.pdf

Life time expectancy	Useful life time: > 100 000 h at U_{NDC} and 70 °C FIT: < 10 x 10^{-9}/h (10 per 10^9 component h) at 0.5 x U_{NDC}, 40 °C

https://www.vishay.com/docs/28164/mkp1848dcl.pdf

Practical Considerations - Summary

- Covered:
  - What causes overshoots and ringing
    - Transformer design (higher k is better)
    - Parasitic capacitances
  - How to design a perfect snubber to minimize overshoot and ringing
  - How to test your silicon devices if you suspect any component failures
  - Different types of capacitors
  - How different types of capacitors degrade

- You now have all the information to complete your analogue converter design

Thanks! Questions?